POST-QUANTUM CRYPTO: CHALLENGES FOR EMBEDDED APPLICATIONS

Joppe Bos APRIL 2022



SECURE CONNECTIONS FOR A SMARTER WORLD

PUBLIC

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MAKE A PLAN

Armen should create an energency plan analyse checkler

- obtain supplie
- · update personal slocuments
- secure household
- resultable exposortion options/mark
- · graste preservation



CREATE A GO-BAG

Propose supplies obead of a hymome. These can makele

- Additional chatter
- · familial discovery
- · Topod samples



KNOW YOUR WING GUIDANCE

Whether separing for a horizone or executing know your wing or initializations guidance. Firstlinely sheek for updates from leadership and maintain communication with your charof uppropriet.



RECOGNIZE WARNINGS & ALERTS

Age present ways to receive elects. Developed real time der appe. Sign up for marrayeth starts in your mea unif be receive of the Emergency Alex System (EAS) and Weekee, Emergency Alex (MEA), which regulates to vego up.



STAY SAFE

Practice good hygiere and advery measures during any part of a fluorizate evaluation or impact. Near family suindepartition in mond and \$000 be obtaind to contact leadership for suindepart.

POST-QUANTUM CRYPTO FOR EMBEDDED DEVICES?

Outline

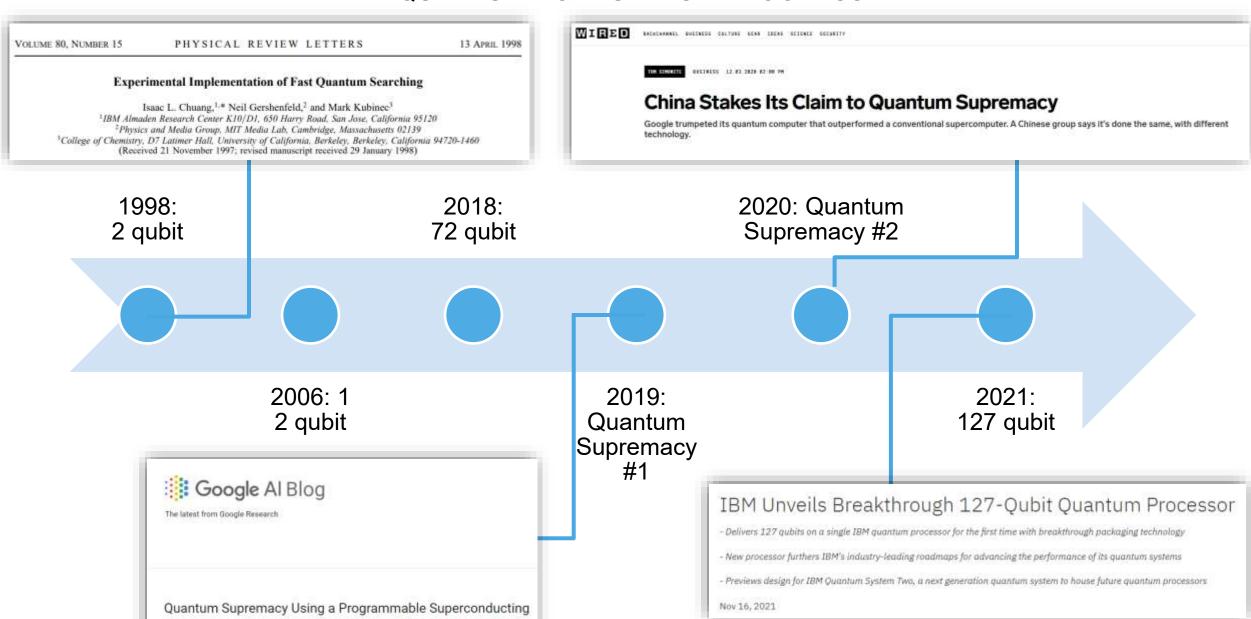
Risk assessment: when to act?

Embedded perspective

- PQC performance
- High-assurance implementations



QUANTUM COMPUTERS - PROGRESS



Processor

Wednesday, October 23, 2019





POST-QUANTUM CRYPTO STANDARDS TIMELINE

2024: NIST Fall 2016: Standard is Call for Jan 2019: Oct. 2020: Round 2 SP 800-208 proposals released Nov. 2017: July 2020: March 2022: Round 3 Deadline for Winners submissions NIST Special Publication 800-208 We are here Recommendation for Stateful **Hash-Based Signature Schemes** Products need to support David A. Cooper **PQC** standard Daniel C. Apon Quynh H. Dang Michael S. Davidson Morris J. Dworkin Carl A. Miller

POST-QUANTUM CRYPTO IS ON THE HORIZON

AUTOMOTIVE

INDUSTRIAL & IOT

MOBILE

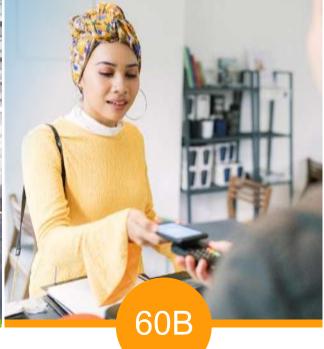
COMMUNICATION INFRASTRUCTURE



70% connected cars by 2025



IoT Edge & end nodes from 6B units in 2021 to 12B units in 2025



Tagging **60B products** per year by 2025



Secure anchors & services for **40B processors**

What is the impact on the billions of embedded devices?



TYPICAL EXAMPLES

Automotive

New platform designed now will likely enter the market after 2024 and remain in use for many years

(Industrial) IoT

Devices sold now need to be able to support the new PQC standard in 2024: crypto agility

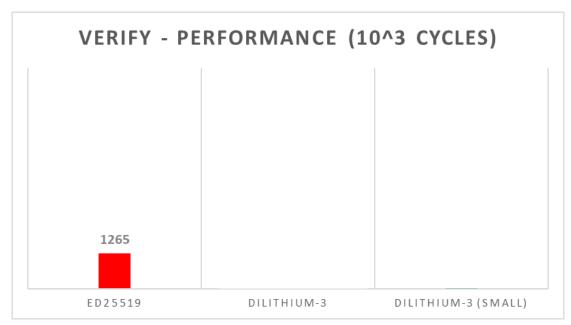
Many embedded IoT platforms are resource constrained: 4-16 KiB memory

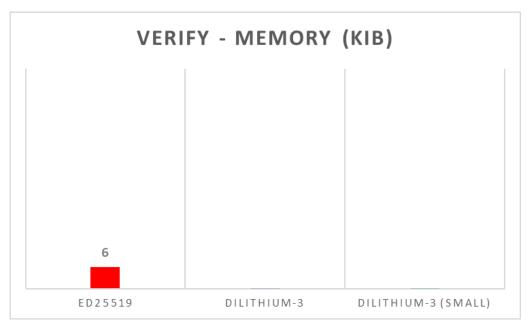




SIGNATURE VERIFICATION - ECC VERSUS PQC

Academic figures on ARM Cortex-M4





Typical crypto operation: signature verification

- Secure boot
- Secure (over-the-air) update

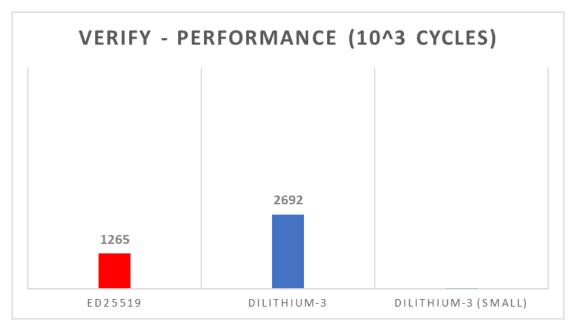
Size (bytes)	Ed25519	Dilithium-3
Private key	64	4000
Public key	32	1952
Signature	64	3293

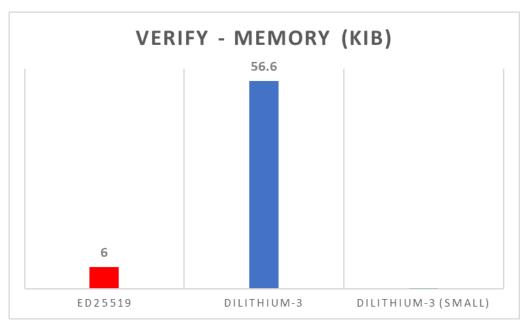
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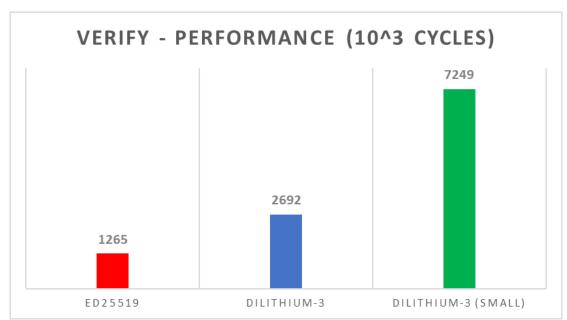
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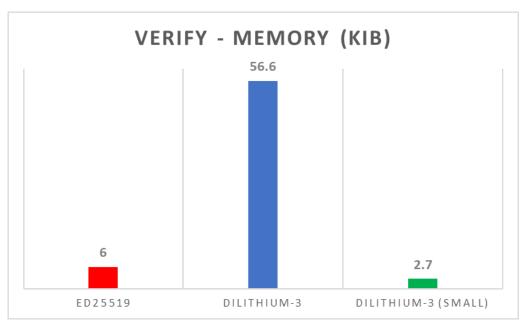
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- Dilithium-3 numbers from Abdulrahman, Hwang, Kannwischer, Sprenkels: Faster Kyber and Dilithium on the Cortex-M4. Cryptology ePrint Archive, Report 2022/112



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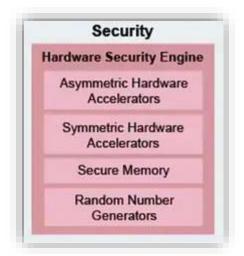
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- Bos, Renes, Sprenkels: Dilithium for Memory Constrained Devices. Cryptology ePrint Archive, Report 2022/323

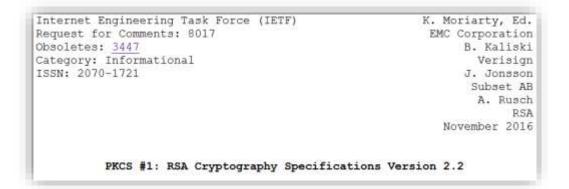


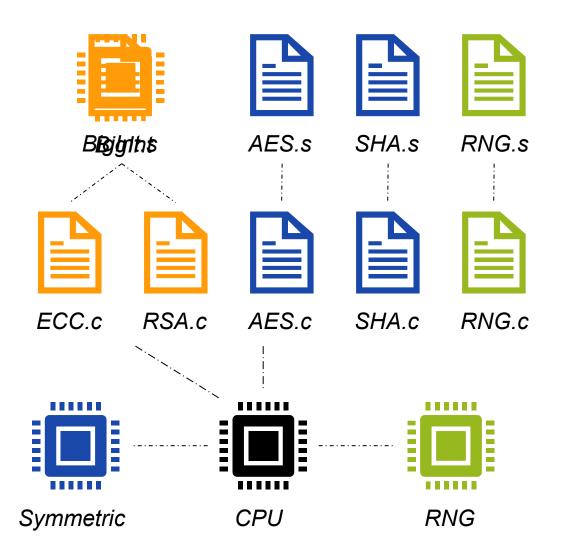
IMPLEMENTING CLASSICAL CRYPTOGRAPHY



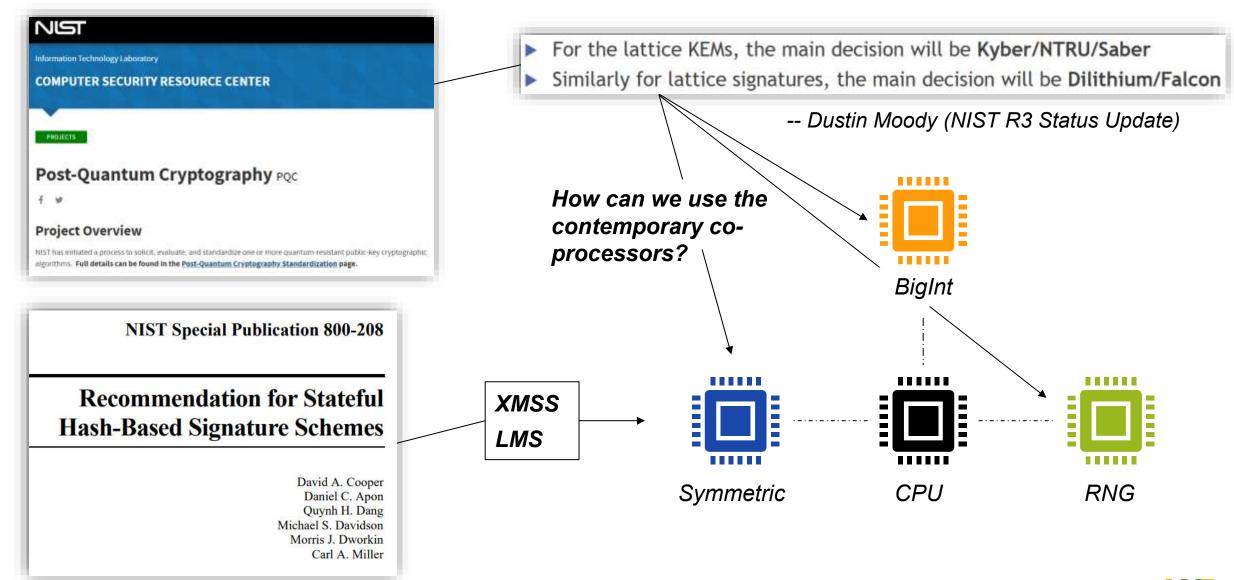


S32G2 automotive processor spec





IMPLEMENTING POST-QUANTUM CRYPTOGRAPHY



REUSING EXISTING COPROCESSORS



Approach	Core	Structure	Size	
RSA	Modular multiplication	$(\mathbb{Z}/n\mathbb{Z})^*$	<i>n</i> is 3072-bit	
ECC	Elliptic curve scalar multiplication	$\mathbb{E}(\mathbb{F}_p)$	p is 256-bit	
Lattice	Polynomial multiplication	$(\mathbb{Z}/q\mathbb{Z})[X]/(X^n+1)$	q is 16-bit n is 256	

Lattice cryptography uses 16-bit coefficients, how to use our bignum coprocessors?

Proposal from [A] for 128-bit coprocessors

Pack multiple 16-bit coefficients in large 128-bit register

Ensure sufficient "space" is reserved to avoid overflow

[A] Albrecht, Hanser, Hoeller, Pöppelmann, Virdia, Wallner: Implementing RLWE-based schemes using an RSA co-processor. TCHES 2019

KRONECKER SUBSTITUTION: POLYNOMIAL MULTIPLICATION WITH INTEGER MULTIPLIERS

Polynomial domain

$$f = 1 + 2x + 3x^2 + 4x^3$$

$$g = 5 + 6x + 7x^2 + 8x^3$$

Grundzüge einer arithmetischen Theorie der algebraischen Grössen.

(Von L. Kronecker.)

(Abdruck einer Festschrift zu Herrn E. E. Kummers Doctor-Jubiläum, 10. September 1881.)



$$fg = 5 + 16x + 34x^2 + 60x^3 + 61x^4 + 52x^5 + 32x^6$$

Kronecker domain (with evaluation point 100)

$$f(100) = 4030201$$

$$g(100) = 8070605$$



$$fg(100) = 32526160341605$$



REUSING EXISTING COPROCESSORS



Lattice

Polynomial multiplication

 $(\mathbb{Z}/q\mathbb{Z})[X]/(X^n+1)$

q is 16-bit *n* is 256

Can we do better?

- Exploit ring properties: Combine Schönhage-Strassen with Kronecker
- Use the roots of unity modulo $X^n + 1$ to construct fast **symbolic** NTTs (as in Nussbaumer)

*Harvey. Faster polynomial multiplication via multipoint Kronecker substitution. J. Sym. Comp. 2009. New: Bos, Renes and Vredendaal: Polynomial Multiplication with Contemporary Co-Processors: Beyond Kronecker, Schönhage-Strassen & Nussbaumer. USENIX Security Symposium, 2022.

9

Kronecker

New

New

1 x 8192-bit multiplication	
2 x 4096-bit multiplication	
4 x 2048-bit multiplication	
8 x 1024-bit multiplication	
16 x 512-bit multiplication	

4096 x 128-bit multiplications 2048 x 128-bit multiplications 1024 x 128-bit multiplications 512 x 128-bit multiplications 256 x 128-bit multiplications



RUNNING PQC ON EMBEDDED DEVICES

Key sizes

Many current embedded devices struggle with RSA-3072 keys
 → PQC is order of magnitude larger

Performance

- Not always as bad as people think.
 - → Dilithium verification (secure boot, update) "only" 1x 3x slower
- Notable disadvantages: <u>variable</u> signing time in Dilithium: probability run-time twice as slow than average is <u>14 percent</u>
- Possibility to re-use existing hardware to accelerate lattice-based crypto

Memory usage

- Many schemes use a lot of stack by default (50 100 KiB).
 - → Dedicated techniques needed



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What about high security implementation?



FO-CALYPSE



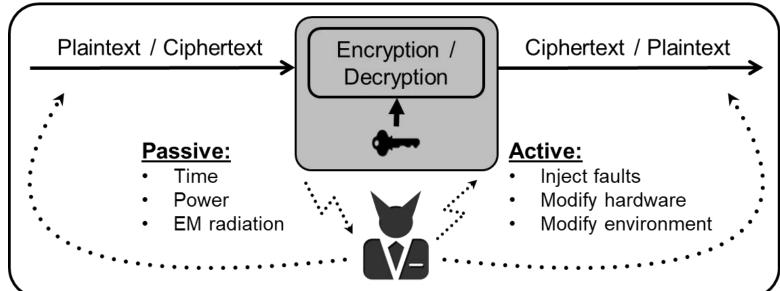
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High-assurance implementations

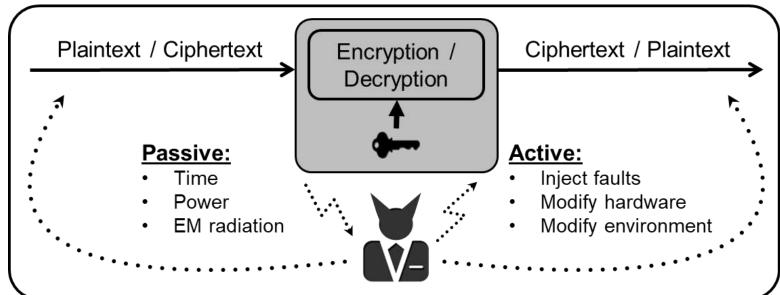


Use meta-information to extract information about the key used in your target platform / product. Many powerful techniques:

fault injections, simple power analysis, differential power analysis, correlation power analysis, template attacks, higher-order correlation attacks, mutual information analysis, linear regression analysis, horizontal analysis, etc



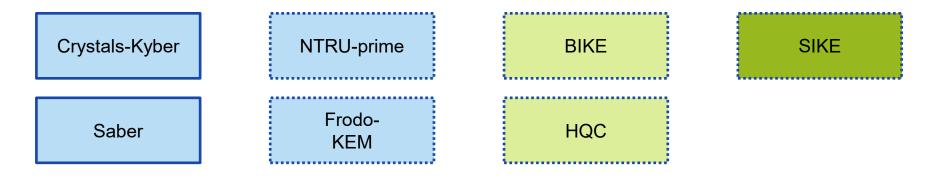
High-assurance implementations



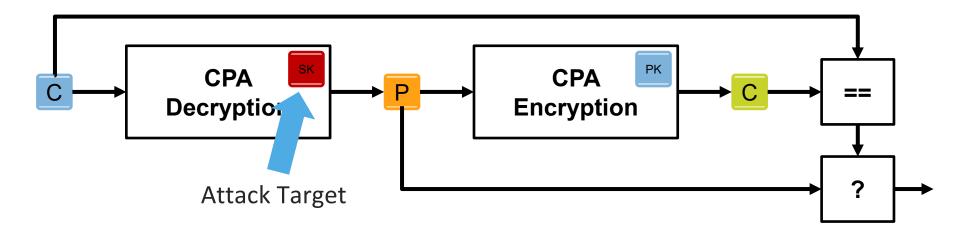
It took many years to find secure and fast protections for RSA + ECC → still cat-and-mouse game

What about Post-Quantum Cryptography?

The Fujisaki-Okamoto (FO) transformation (or slight variants) underlies the IND-CCA security of many KEMs, e.g.:

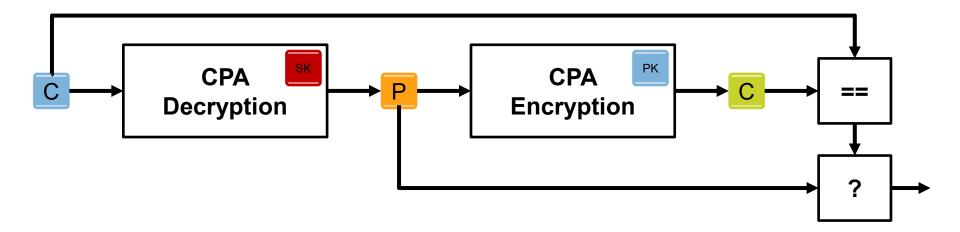


Exemplary Decapsulation:



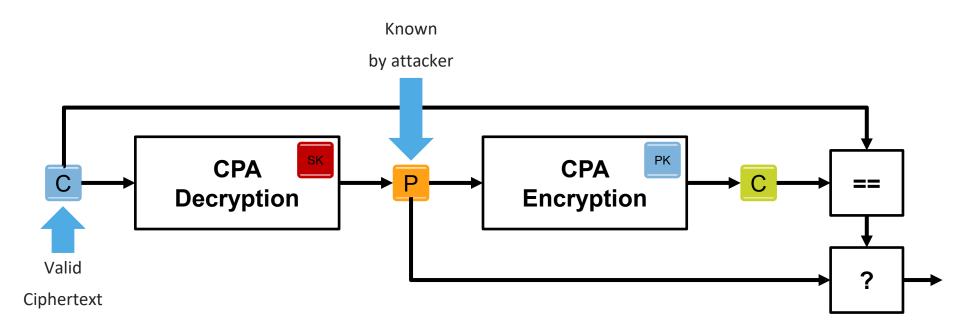
Attack 1: Chosen Plaintext

Attacker inputs only valid ciphertexts



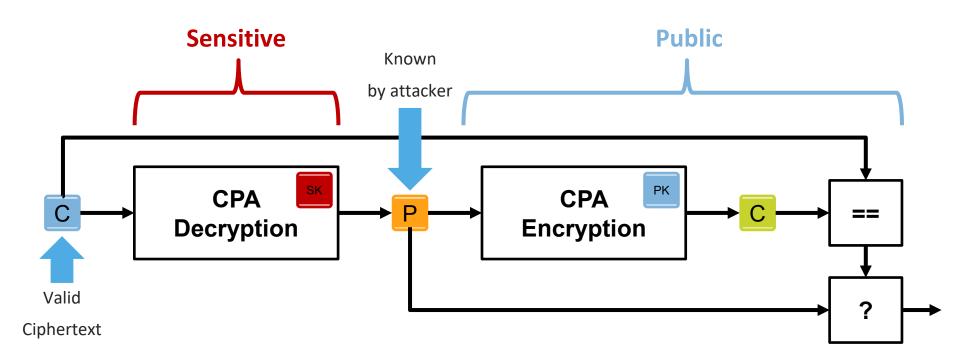
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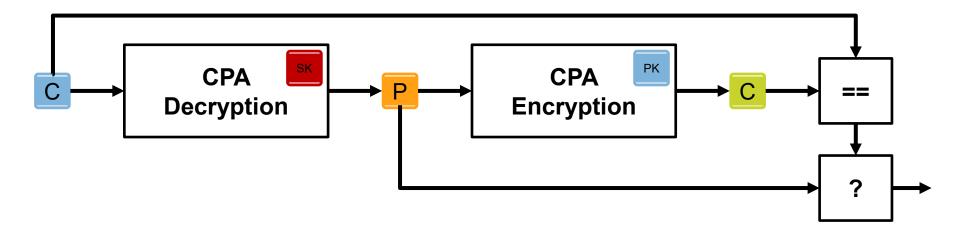
Attack 1: Chosen Plaintext

- Attacker inputs only valid ciphertexts
- Attack focuses on **CPA Decryption**, everything after (and including) P is public
- Only need to protect CPA Decryption



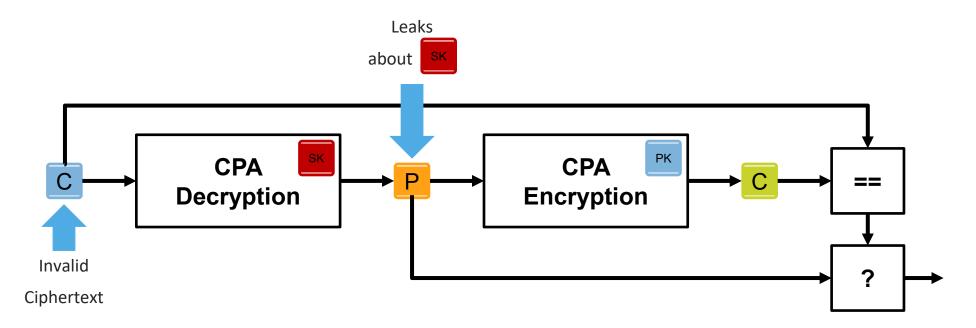
Attack 2: Chosen Ciphertext

• Attacker inputs specially-crafted invalid ciphertexts



Attack 2: Chosen Ciphertext

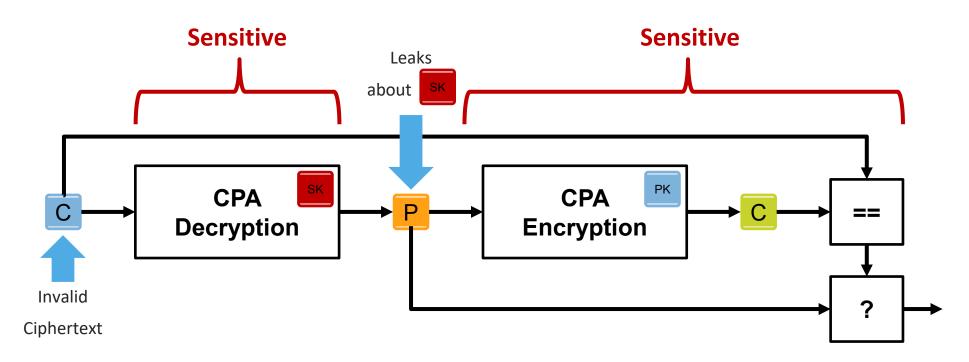
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Attack 2: Chosen Ciphertext

- Attacker inputs specially-crafted invalid ciphertexts
- Attack focuses on **CPA Decryption** + everything after (and including) P is potentially sensitive
- Potentially all (or most) modules need to be hardened







Why is it bad?



Millions of Points of Interest (Pol)

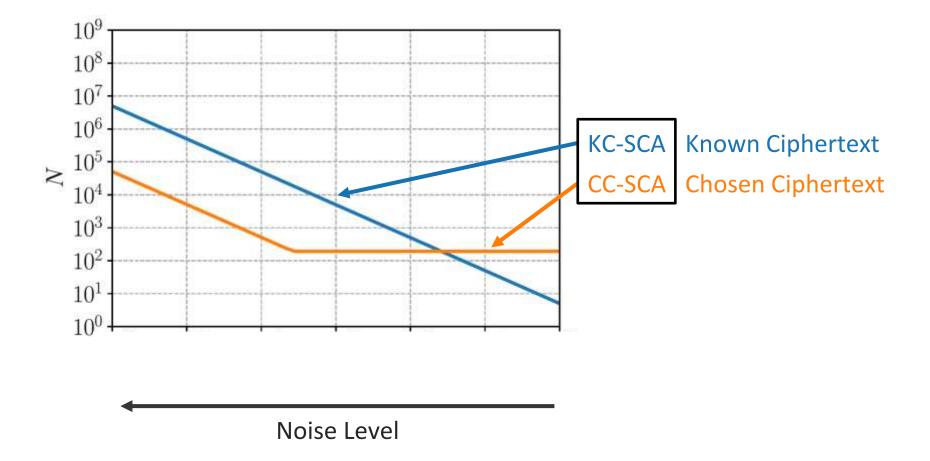
Most recently at TCHES-2022:

Masked Kyber / Saber is broken with only 15k traces.

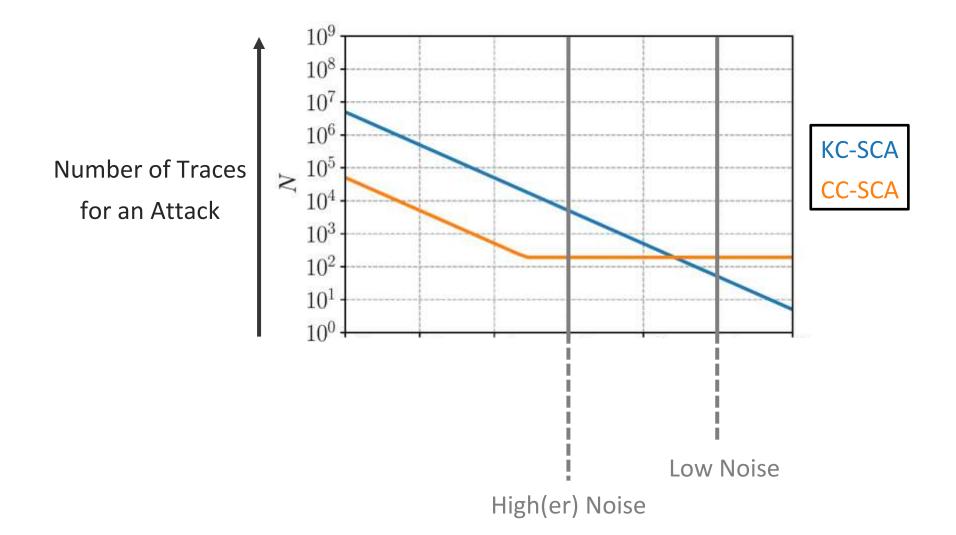
Curse of Re-encryption: A Generic Power/EM Analysis on Post-Quantum KEMs

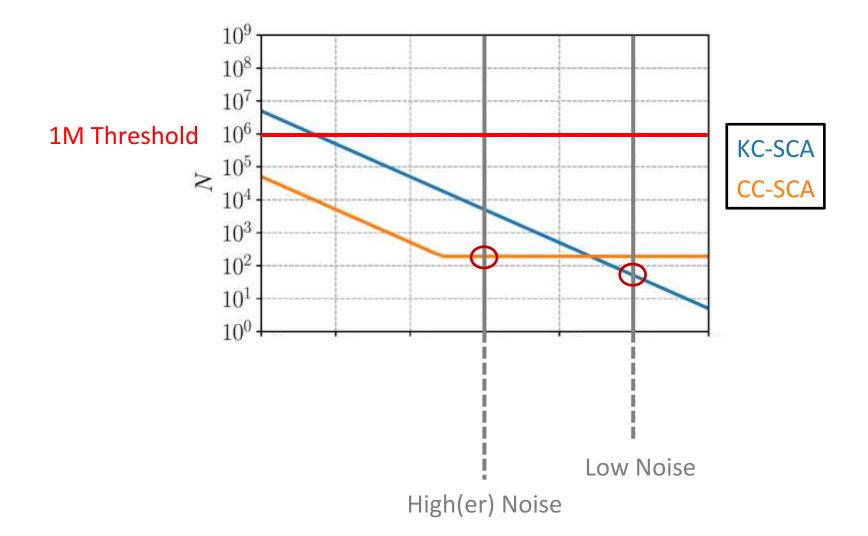
Rei Ueno^{1,2,3}, Keita Xagawa⁴, Yutaro Tanaka^{1,2}, Akira Ito^{1,2}, Junko Takahashi⁴ and Naofumi Homma^{1,2}

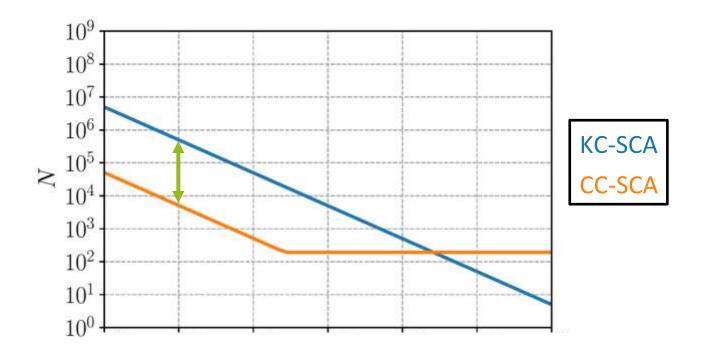




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- Unprotected Kyber is (unsurprisingly) not sufficient for both noise levels
- There is a gap of roughly **x100** between the attacks for high(er) noise



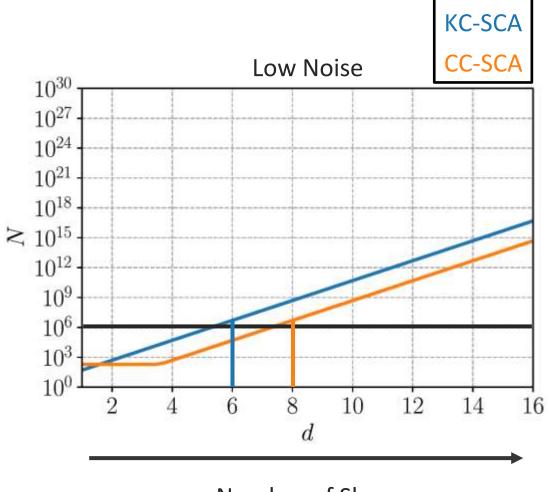
Can this be overcome through masking?

CASE STUDY: MASKED KYBER

Split variables into *d* shares.

Higher *d* = Higher security + Increased cost

Pre-Quantum: Certified industrial solutions **d = 2-3**



Number of Shares



CASE STUDY: MASKED KYBER

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Higher *d* = Higher security + Increased cost

Pre-Quantum: Certified industrial solutions **d = 2-3**

For **low noise**:

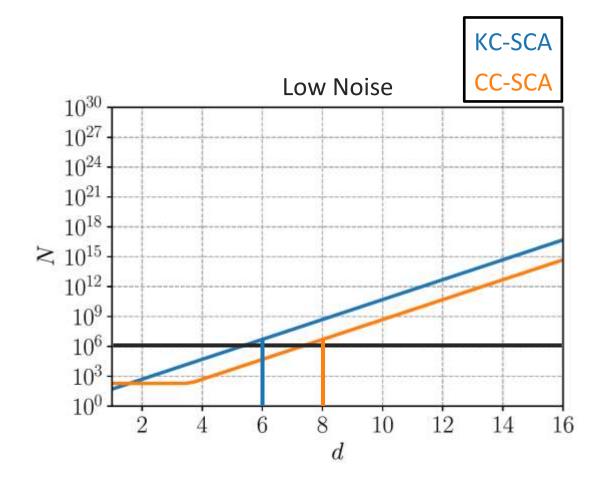
- Known ciphertext \rightarrow d = 6
- Chosen ciphertext → d = 8

FO leakage causes an increase of **2** shares.

For high(er) noise:

- Known ciphertext \rightarrow d = 2
- Chosen ciphertext → d = 3

FO leakage causes an increase of **1** share.





Higher-Order Masking

Case Study: Higher-order masked Kyber (M4) from [BGR+21]

(with adapted A2B)

Overhead compared to unprotected (d=1):

d=2	d=3	d=4	d=5	d=6	d=7
3.5x	64x	110x	197x	293x	397x



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d=2	d=3	d=4	d=5	d=6	d=7	N1 / A *
3.5x	64x	110x	197x	293x	397x	N/A*
18x	High(er)				?	Low

* For this specific implementation + board.

Requires further stack usage optimization.



Leakage caused by the FO significantly increases deployment costs of affected KEMs



Alternative Solution: Encrypt-then-Sign KEM

Replace FO check by **signature verification** for some use cases

- Uses less shares because no FO leakage
- Verification only with public values (no SCA protection)

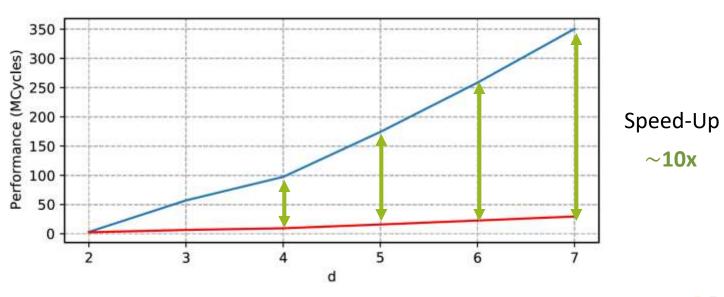


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Example: Kyber + Dilithium







CONCLUSIONS

<u>Irrelevant</u> if the quantum threat is real or not New PQC-Standard are coming!

→ Post-quantum crypto is already being requested

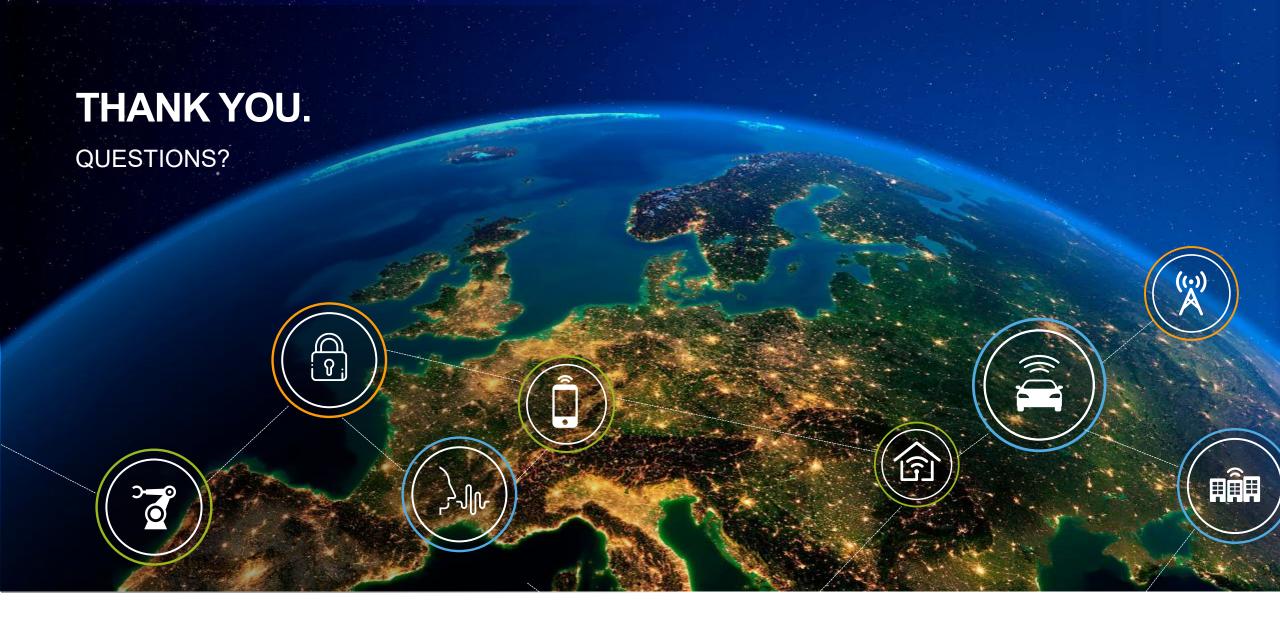
For embedded platforms challenges in terms of

- Performance, memory and key-sizes
- How to efficiently achieve protection against sophisticated side-channel attacks?

- ✓ Think about migration paths now
- ✓ Exciting times to work on crypto & security solutions!

CONTACT: PQC@NXP.COM | NXP.COM/PQC









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